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April 3, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject: Serial No. 10/056,978 01/25/02

Yue-Der Chih et al.

METHOD OF MARGINAL ERASURE FOR THE TESTING OF FLASH MEMORIES

Grp. Art Unit: 2818

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on April 10, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 4/10/02

The following two U.S. Patents describe methods for post-package testing of one-time-programmable (OTP) EPROM memories where cells are marginally programmed to demonstrate that they are addressable:

1) U.S. Patent 4,809,231 to Shannon et al., "Method and Apparatus for Post-Packaging Testing of One-Time Programmable Memories."
2) U.S. Patent 4,903,265 to Shannon et al., "Method and Apparatus for Post-Packaging Testing of One-Time Programmable Memories."

U.S. Patent 5,142,495 to Canepa, "Variable Load for Margin Mode," teaches a margining circuit in an EPROM where a plurality of parallel transistors form a variable load.

U.S. Patent 5,369,616 to Wells et al., "Method for Assuring that an Erase Process for a Memory Array has been Properly Completed," teaches a method where non-volatile memory is used to set memory system parameters such as threshold, word length, and addressing scheme.

U.S. Patent 5,544,116 to Chao et al., "Erase and Program Verification Circuit for Non-Volatile Memory," teaches a method of verifying program states of Flash EPROM cells where different voltages are applied to the reference and memory cells.

U.S. Patent 5,675,537 to Bill et al., "Erase Method for Page Mode Multiple Bits-per-Cell Flash EEPROM," teaches a method where overerasure of memory cells in a Flash EPROM is prevented by halting erasure once a prescribed cell threshold is reached.

U.S. Patent 5,870,407 to Hsia et al., "Method of Screening Memory Cells at Room Temperature that would be Rejected During Hot Temperature Programming Tests," teaches a method of predicting high temperature failures of Flash EPROM memory devices that reduces testing time and packaging cost.

U.S. Patent 6,122,198 to Haddad et al., "Bit by Bit APDE Verify for Flash Memory Applications," teaches a method for guaranteeing that an erased cell threshold voltage in a two bit per cell Flash EPROM falls within prescribed limits.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761